

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and the first and second silicon wafers are effectively a bonded together set of wafers.

2. The method of claim 1, further comprising: placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

3. The method of claim 2, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

4. The method of claim 3, further comprising coating the second wafer with antireflection material.

5. The method of claim 4, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8-14 micron wavelength region of light going through the second silicon wafer to the plurality of devices.

6. The method of claim 5, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

7. The method of claim 6, wherein the plurality of devices comprise thermoelectric detectors.

8. The method of claim 6, wherein the plurality of devices comprise bolometers.

9. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

- growing a first thermal layer on a first side of a first silicon wafer;
- depositing a nitride layer on the first thermal layer;
- depositing and patterning a first metal layer on the nitride layer for at least one device;
- depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;
- patterned and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a pump-out port through the first silicon wafer and the layers on the first silicon wafer;
- masking and removing material from a first side of a second silicon wafer, to form a recess in the first side of the second silicon wafer;
- forming a sealing ring on the first side of the second silicon wafer around the recess; and
- positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

the sealing ring is in contact with at least one of the layers on the first side of the first silicon layer;

the at least one device is within the recess resulting in a chamber containing the at least one device;

the pump-out port is within the sealing ring; and

the first and second silicon wafers are effectively a bonded together set of wafers.

10. The method of claim 9, further comprising:

placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the pump-out port on the second

side of the first silicon wafer, wherein the chamber is sealed from the environment.

11. The method of claim 10, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first silicon wafer.

12. The method of claim 11, wherein the at least one device is a detector.

13. The method of claim 12, further comprising coating the second silicon wafer with antireflection material.

14. The method of claim 11, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8-14 micron wavelength region of light going through the second silicon wafer to the at least one device.

15. The method of claim 14, wherein the at least one device is a thermoelectric detector.

16. The method of claim 14, wherein the at least one device is a bolometer.

17. The method of claim 11, wherein the at least one device is an emitter.

18. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

- growing a first layer of thermal  $\text{SiO}_2$  on a first side of a first silicon wafer;
- depositing a first layer of  $\text{Si}_3\text{N}_4$  on the first layer of thermal  $\text{SiO}_2$ ;
- growing a second layer of thermal  $\text{SiO}_2$  on a second side of the first silicon wafer;
- depositing a second layer of  $\text{Si}_3\text{N}_4$  on the second layer of thermal  $\text{SiO}_2$ ;
- depositing a layer of a first metal on the second layer of  $\text{Si}_3\text{N}_4$ ;
- patterning the layer of the first metal;
- depositing a layer of a second metal on the layer of the first metal;
- patterning the layer of the second metal;
- depositing a third layer of  $\text{Si}_3\text{N}_4$  on the layers of the first and second metals;
- etching at least one via through the third layer of  $\text{Si}_3\text{N}_4$ , the layers of the second and first metals, the second layer of  $\text{Si}_3\text{N}_4$  and the second layer of thermal  $\text{SiO}_2$ ;
- etching a pump-out port through the first layer of  $\text{SiO}_2$  and a first portion of the silicon wafer proximate to the at least one via;
- etching within the at least one via through a second portion of the silicon wafer to the pump-out port;
- growing a third layer of thermal  $\text{SiO}_2$  on a first side of a second silicon wafer and a fourth layer of thermal  $\text{SiO}_2$  on a second side of the second silicon wafer;
- growing a fourth layer of  $\text{Si}_3\text{N}_4$  on the third layer of thermal  $\text{SiO}_2$  and a fifth layer of  $\text{Si}_3\text{N}_4$  on the fourth layer of  $\text{SiO}_2$ ;
- patterning and cutting the fourth layer  $\text{Si}_3\text{N}_4$  and the third layer of thermal  $\text{SiO}_2$  for a bond pad area;
- etching a first portion of the second silicon wafer through the fourth  $\text{Si}_3\text{N}_4$  layer and third  $\text{SiO}_2$  layer for the bond pad area;
- patterning and cutting the fifth layer of  $\text{Si}_3\text{N}_4$  and fourth layer of thermal  $\text{SiO}_2$  for a recess area;
- etching a second portion from the second side of the second silicon wafer to form a recess;
- applying an optical coating to the second silicon wafer to substantially reduce reflections;

applying a solder ring proximate to a perimeter of the recess, on the second side of the second silicon wafer; aligning the first silicon wafer with the second silicon wafer, having the first side of the first silicon wafer and the second side of the second silicon wafer face each other;

putting the first and second silicon wafers in a vacuum; pressing the first and second silicon wafers together with a pressure;

ramping the temperature of the silicon wafers up to a high temperature;

increasing the pressure of the first and second silicon wafers against each other to bond the silicon wafers to each other;

baking out the first and second silicon wafers;

cooling down the first and second silicon wafers under a maintained vacuum;

depositing a layer of a metal on the second side of the second silicon wafer to plug the pump-out port to seal the recess with a vacuum; and

removing the bonded first and second silicon wafers from the vacuum.

19. A method for making a wafer-pair having deposited 25 layer plugged sealed chambers, comprising:

growing a thermal layer on a first side of a first silicon wafer;

patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a plurality of pump-out ports through the first silicon wafer and layers on the first silicon wafer;

masking and removing material from a first side of a second silicon wafer to form a plurality of recesses in 35 the first side of the second silicon wafer;

forming a sealing ring on the first side of the second silicon wafer around each of the plurality of recesses; and

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first silicon layer; each recess of the plurality of recesses results in a chamber;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and the first and second silicon wafers are effectively a bonded together set of wafers.

20. The method of claim 19, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

21. The method of claim 20, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

22. The method of claim 21, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

23. The method of claim 22, wherein the one or more sealed chambers contains one or more devices.

24. The method of claim 19, further comprising: placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from an ambient environment.

\* \* \* \* \*

*Add A >*

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100  
101  
102  
103  
104  
105  
106  
107  
108  
109  
110  
111  
112  
113  
114  
115  
116  
117  
118  
119  
120  
121  
122  
123  
124  
125  
126  
127  
128  
129  
130  
131  
132  
133  
134  
135  
136  
137  
138  
139  
140  
141  
142  
143  
144  
145  
146  
147  
148  
149  
150  
151  
152  
153  
154  
155  
156  
157  
158  
159  
160  
161  
162  
163  
164  
165  
166  
167  
168  
169  
170  
171  
172  
173  
174  
175  
176  
177  
178  
179  
180  
181  
182  
183  
184  
185  
186  
187  
188  
189  
190  
191  
192  
193  
194  
195  
196  
197  
198  
199  
200  
201  
202  
203  
204  
205  
206  
207  
208  
209  
210  
211  
212  
213  
214  
215  
216  
217  
218  
219  
220  
221  
222  
223  
224  
225  
226  
227  
228  
229  
230  
231  
232  
233  
234  
235  
236  
237  
238  
239  
240  
241  
242  
243  
244  
245  
246  
247  
248  
249  
250  
251  
252  
253  
254  
255  
256  
257  
258  
259  
259  
260  
261  
262  
263  
264  
265  
266  
267  
268  
269  
270  
271  
272  
273  
274  
275  
276  
277  
278  
279  
280  
281  
282  
283  
284  
285  
286  
287  
288  
289  
290  
291  
292  
293  
294  
295  
296  
297  
298  
299  
300  
301  
302  
303  
304  
305  
306  
307  
308  
309  
310  
311  
312  
313  
314  
315  
316  
317  
318  
319  
320  
321  
322  
323  
324  
325  
326  
327  
328  
329  
330  
331  
332  
333  
334  
335  
336  
337  
338  
339  
340  
341  
342  
343  
344  
345  
346  
347  
348  
349  
350  
351  
352  
353  
354  
355  
356  
357  
358  
359  
360  
361  
362  
363  
364  
365  
366  
367  
368  
369  
370  
371  
372  
373  
374  
375  
376  
377  
378  
379  
380  
381  
382  
383  
384  
385  
386  
387  
388  
389  
390  
391  
392  
393  
394  
395  
396  
397  
398  
399  
400  
401  
402  
403  
404  
405  
406  
407  
408  
409  
410  
411  
412  
413  
414  
415  
416  
417  
418  
419  
420  
421  
422  
423  
424  
425  
426  
427  
428  
429  
430  
431  
432  
433  
434  
435  
436  
437  
438  
439  
440  
441  
442  
443  
444  
445  
446  
447  
448  
449  
450  
451  
452  
453  
454  
455  
456  
457  
458  
459  
460  
461  
462  
463  
464  
465  
466  
467  
468  
469  
470  
471  
472  
473  
474  
475  
476  
477  
478  
479  
480  
481  
482  
483  
484  
485  
486  
487  
488  
489  
490  
491  
492  
493  
494  
495  
496  
497  
498  
499  
500  
501  
502  
503  
504  
505  
506  
507  
508  
509  
510  
511  
512  
513  
514  
515  
516  
517  
518  
519  
520  
521  
522  
523  
524  
525  
526  
527  
528  
529  
530  
531  
532  
533  
534  
535  
536  
537  
538  
539  
540  
541  
542  
543  
544  
545  
546  
547  
548  
549  
550  
551  
552  
553  
554  
555  
556  
557  
558  
559  
559  
560  
561  
562  
563  
564  
565  
566  
567  
568  
569  
569  
570  
571  
572  
573  
574  
575  
576  
577  
578  
579  
579  
580  
581  
582  
583  
584  
585  
586  
587  
588  
589  
589  
590  
591  
592  
593  
594  
595  
596  
597  
598  
599  
599  
600  
601  
602  
603  
604  
605  
606  
607  
608  
609  
609  
610  
611  
612  
613  
614  
615  
616  
617  
618  
619  
619  
620  
621  
622  
623  
624  
625  
626  
627  
628  
629  
629  
630  
631  
632  
633  
634  
635  
636  
637  
638  
639  
639  
640  
641  
642  
643  
644  
645  
646  
647  
648  
649  
649  
650  
651  
652  
653  
654  
655  
656  
657  
658  
659  
659  
660  
661  
662  
663  
664  
665  
666  
667  
668  
669  
669  
670  
671  
672  
673  
674  
675  
676  
677  
678  
679  
679  
680  
681  
682  
683  
684  
685  
686  
687  
688  
689  
689  
690  
691  
692  
693  
694  
695  
696  
697  
698  
699  
699  
700  
701  
702  
703  
704  
705  
706  
707  
708  
709  
709  
710  
711  
712  
713  
714  
715  
716  
717  
718  
719  
719  
720  
721  
722  
723  
724  
725  
726  
727  
728  
729  
729  
730  
731  
732  
733  
734  
735  
736  
737  
738  
739  
739  
740  
741  
742  
743  
744  
745  
746  
747  
748  
749  
749  
750  
751  
752  
753  
754  
755  
756  
757  
758  
759  
759  
760  
761  
762  
763  
764  
765  
766  
767  
768  
769  
769  
770  
771  
772  
773  
774  
775  
776  
777  
778  
779  
779  
780  
781  
782  
783  
784  
785  
786  
787  
788  
789  
789  
790  
791  
792  
793  
794  
795  
796  
797  
798  
799  
799  
800  
801  
802  
803  
804  
805  
806  
807  
808  
809  
809  
810  
811  
812  
813  
814  
815  
816  
817  
818  
819  
819  
820  
821  
822  
823  
824  
825  
826  
827  
828  
829  
829  
830  
831  
832  
833  
834  
835  
836  
837  
838  
839  
839  
840  
841  
842  
843  
844  
845  
846  
847  
848  
849  
849  
850  
851  
852  
853  
854  
855  
856  
857  
858  
859  
859  
860  
861  
862  
863  
864  
865  
866  
867  
868  
869  
869  
870  
871  
872  
873  
874  
875  
876  
877  
878  
879  
879  
880  
881  
882  
883  
884  
885  
886  
887  
888  
889  
889  
890  
891  
892  
893  
894  
895  
896  
897  
898  
899  
899  
900  
901  
902  
903  
904  
905  
906  
907  
908  
909  
909  
910  
911  
912  
913  
914  
915  
916  
917  
918  
919  
919  
920  
921  
922  
923  
924  
925  
926  
927  
928  
929  
929  
930  
931  
932  
933  
934  
935  
936  
937  
938  
939  
939  
940  
941  
942  
943  
944  
945  
946  
947  
948  
949  
949  
950  
951  
952  
953  
954  
955  
956  
957  
958  
959  
959  
960  
961  
962  
963  
964  
965  
966  
967  
968  
969  
969  
970  
971  
972  
973  
974  
975  
976  
977  
978  
979  
979  
980  
981  
982  
983  
984  
985  
986  
987  
988  
989  
989  
990  
991  
992  
993  
994  
995  
996  
997  
998  
999  
999  
1000